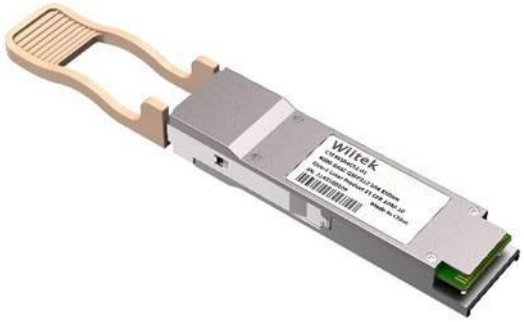
QSFP112 400G SR4 Optical Transceiver

Product Specifications

Wiitek's 400G QSFP112 SR4 transceiver is designed for use in 400G Ethernet links up to 100m over OM4/OM5 and 60m over OM3 multi-mode fiber. The module converts 4 channels of 100Gb/s (PAM4) electrical input data to 4 channels of parallel optical signals, each capable of 100Gb/s operation for an aggregate data rate of 400Gb/s.

On the receiver side, the module converts 4 channels of parallel optical signals of 100Gb/s each channel for an aggregate data rate of 400Gb/s into 4 channels of 100Gb/s (PAM4) electrical output data.

An optical fiber cable with an MPO12-APC connector can be plugged into the QSFP112 SR4 module receptacle. Host FEC is required to support up to OM4/OM5 100m fiber transmission.



Features

- Compliant to QSFP112 MSA V2.0
- Compliant with CMIS 4.0
- Parallel 4 Optical Lanes
- IEEE 802.3db 400GBASE-SR4 Specification compliant
- 4x106. 25Gb/s electrical interface (400GAUI-4)
- Up to 100m over Om4/OM5 and 60m over OM3
- Maximum power consumption 8W
- MPO12-APC Receptacle
- Single +3.3V power supply
- Case temperature range: 0 ~ +70℃
- RoHS 2.0 complaint

Applications

- 400G Ethernet
- Data Center Interconnect
- Enterprise Networking

Rev	Date	Modified by	Description
A	Aug 17,2022	David	Initial Release
B	Nov 12,2022	Vic	Updated Maximum power
C	Mar 8,2024	Vic	Updated describe
D	Oct 20,2024	Vic	Update product information

1. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Storage Temperature Range	T_{STG}	-40	+85	°C
Supply Voltage	V_{CC}	-0.5	3.6	V
Relative Humidity	RH	5% to 95% non-condensing		

2. Operating Conditions

Parameter	Symbol	Min	Max	Unit
Case Temperature- Operating	T_{CASE}	0	70	°C
Supply Voltage	Vcc	3.135	3.465	V
Power Consumption	P_{DISS}		8	W
Pre-FEC Bit Error Ratio			$2.4x10^{-4}$	
Link Distance over OM3		0.5	60	M
Link Distance over OM4		0.5	100	M

3. Transmitter Optical Specifications

Transmitter Parameter	Min	Typical	Max	Unit
Signaling rate each lane		53.125±100ppm		GBd
Lane Wavelength Range		850		nm
RMS Spectral width			0.6	nm
Modulation Format		PAM4		
Average Optical Power per lane	-4.6		4	dBm
Outer Optical Modulation Amplitude (OMAouter), each lane for TDECQ<=1.8dB for 1.8<TDECQ<=4.4dB	 -2.6 -4.4+TDECQ		 3.5 3.5	dBm
Outer Optical Modulation Amplitude (OMAouter), each lane for TECQ<=1.8dB for 1.8<TECQ<=4.4dB	 -2.6 -4.4+TDECQ		 3.5 3.5	dBm
Transmitter and Dispersion Eye Closure for PAM4, each Lane			4.4	dB
Transmitter Eye Closure for PAM4(TECQ), each Lane			4.4	dB
Extinction Ratio	2.5			dB
Tranmitter excursion ,each lane			2	dB
Trasmitter transition time,each lane			17	ps
Average Launch Power per Lane @ TX Off State			-30	dBm
Relative Intensity $Noise_{14}$(OMA)			-132	dB/Hz
Optical Return Loss Tolerance			14	dB
Encircled Flux		>=86% at 19um <=30% at 4.5um		-

4. Receiver Optical Specifications

Receiver Parameter	Min	Typical	Max	Unit
Signaling rate each lane		53.125±100ppm		GBd
Lane Wavelength Range		850		nm
Modulation Format		PAM4		
Damage Threshold	5			dBm
Average Receive Power, each lane	-6.4		4	dBm
Receiver Power, each lane (OMA)			3.5	dBm
Receiver Sensitivity each lane (OMA_{outer}) for TECQ<=1.8dB for 1.8<TECQ<=4.4dB			 -4.6 -6.4+TECQ	dBm
Receiver reflectance			-15	dB
Stressed Receiver Sensitivity (OMA_{outer}), each			-2	dBm
Stressed Conditions for Stress Receiver Sensitivity				
Stressed Eye Closure for PAM4 (SECQ),Lane under Test		4.4		dB
OMAouter of each Aggressor Lane		3.5		dBm

5. Receiver Thresholds for Loss of Signal (LOS)

Parameter	Min	Typical	Max	Unit
RX_LOS_Assert Min/Max	-15.0			dBm
RX_LOS_De-Assert Min/Max			-8.9	dBm
RX_LOS_Hysteresis		1.5		dB

6.Digital Diagnostic Monitoring Specifications

Parameters	Unit	Specification
Temperature Monitor absolute error	℃	± 3
Supply Voltage Monitor absolute error	%	± 5
I_bias Monitor absolute error	%	± 10
Received Power (Rx) Monitor absolute error	dB	± 3.0
Transmit Power (Tx) Monitor absolute error	dB	± 3.0

7. Low Speed Electrical signal

Parameter	Symbol	Min	Max	Units	Condition
SCL and SDA	VOL	0	0.4	V	IOL(max)=3.0mA for fast mode, 20mA for Fast-mode plus
	VOH	Vcc-0.5	Vcc+0.3	V	
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	Vcc*0.7	Vcc +0.5	V	
Capacitance for SCL and SDA I/O pin	Ci		14	pF	
Total bus cpacitive load for SCL and SDA	Cb		100	pF	3.0k Ohms Pull up resistor, max
			200	pF	1.6k Ohms Pull up resistor, max
LPMode/TxDis,Reset and ModeSeIL	VIL	-0.3	0.8	V	|Iin| </= 125uA for 0V<Vin < Vcc
	VIH	2	Vcc + 0.3	V	
IntL/RxLOS	VOL	0	0.4	V	IOL=2.0mA
	VOH	VCC - 0.5	VCC + 0.3	V	10k ohms pull-up to Host Vcc
ModPrsL	VOL	0	0.4	V	IOL=2.0mA
	VOH				ModPrsL can be implemented as a short-circuit to GND on the module

8. High Speed Electrical signal

Parameter	Min	Typical	Max	Unit	Notes
Receiver electrical output characteristics at TP4					
Signaling rate per lane		53.125		GBd	
AC common-mode output voltage(RMS)		-	17.5	mV	
Differential peak-to-peak output voltage			900	mV	
Near-end Eye height, differential	24			mV	
Near-end vertical eye closure			7.5	dB	
Far-end Eye height, differential	24			mV	
Far-end vertical eye closure			7.5	dB	
Common mode to differential conversion return loss	802.3ck 120G-1				
Effective return loss	8.5			dB	
Differential termination mismatch			10	%	
Transition time (min, 20% to 80%)	8.5			ps	
DC common mode voltage	-350		2850	mV	
Transmitter electrical input characteristics at TP1					
Signaling rate, per lane		53.125		GBd	
Differential pk-pk input voltage tolerance	900			mV	
Common-mode to differential return loss	802.3ck Equation(120G-1)				
Effective return loss	8.5			dB	
Differential termination mismatch			10	%	
Module stressed input test	See 120G.3.4.1				
Single-ended voltage tolerance range	-0.4		3.3	V	
DC common-mode voltage	-350		2850	mV	

9. Module Block Diagram

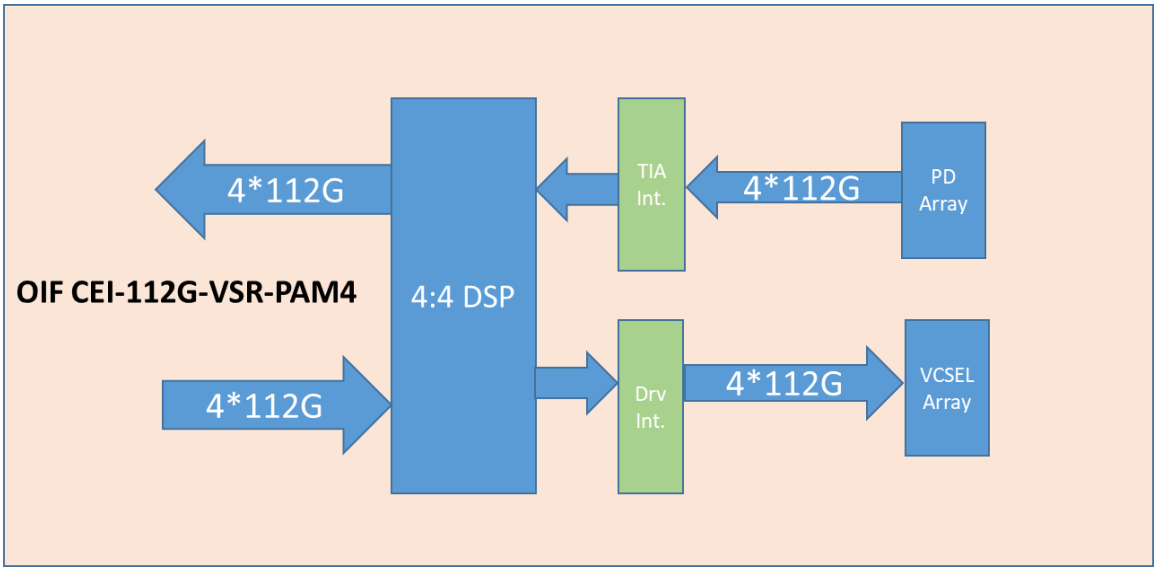


Figure 1. Module Block Diagram

10. QSFP112 Edge Connector and Pinout Description

The electrical pinout of the QSFP112 module is shown in Figure 2 below.

Figure 2. QSFP112 module contact assignment

11. Module contact definition

Pin No.	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	TX2n	Transmitted Inverted Data Input	3	
3	CML-I	TX2p	Transmitted Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	TX4n	Transmitted Inverted Data Input	3	
6	CML-I	TX4p	Transmitted Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSeil	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3 VDC Receiver Power Supply	2	2
11	LVCMOS-I/O	SCL	Serial Clock for I2C Interface	3	
12	LVCMOS-I/O	SDA	Serial Data for I2C Interface	3	
13		GND	Ground	1	1
14	CML-O	RX3p	Receiver Non-Inverted Data Output	3	
15	CML-O	RX3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	RX1p	Receiver Non-Inverted Data Output	3	
18	CML-O	RX1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	RX2n	Receiver Inverted Data Output	3	
22	CML-O	RX2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	RX4n	Receiver Inverted Data Output	3	
25	CML-O	RX4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL/RxLOS	Interrupt/optional RxLOS	3	
29		Vcc Tx	+3.3 VDC Transmitter Power Supply	2	2
30		Vcc1	+3.3 VDC Power Supply	2	2
31	LVTTL-I	LPMode/Tx dis	Low Power Mode/optioanl Tx Disable	3	
32		GND	Ground	1	1
33	CML-I	TX3p	Transmitted Non-Inverted Data Input	3	
34	CML-I	TX3n	Transmitted Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	TX1p	Transmitted Non-Inverted Data Input	3	
37	CML-I	TX1n	Transmitted Inverted Data Input	3	
38		GND	Ground	1	1

Note 1: GND is the symbol for signal and supply (power) common for the QSFP112 module. All are common within the QSFP112 module and all voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements, defined for the host side of the Host Edge Card Connector, are listed in Table 4. Recommended host board power supply filtering is shown in Figure 4. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP112 module in any combination. The connector pins are each rated for a maximum current of 1.5A (max. current of 2.0 A is required for high module power of 15-20W).

12. Optical interface

The four transmit and four receive optical lanes of the module occupy the positions depicted in Figure 3 when looking into the MPO12-APC receptacle with the connector keyway feature on top. The interface contains eight active lanes within twelve total positions. The transmit optical lanes occupy the left-most four positions. The receive optical lanes occupy the right-most four positions. The four center positions are unused.

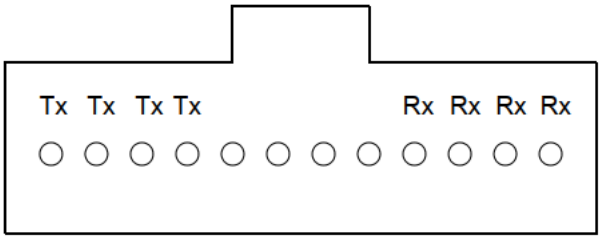
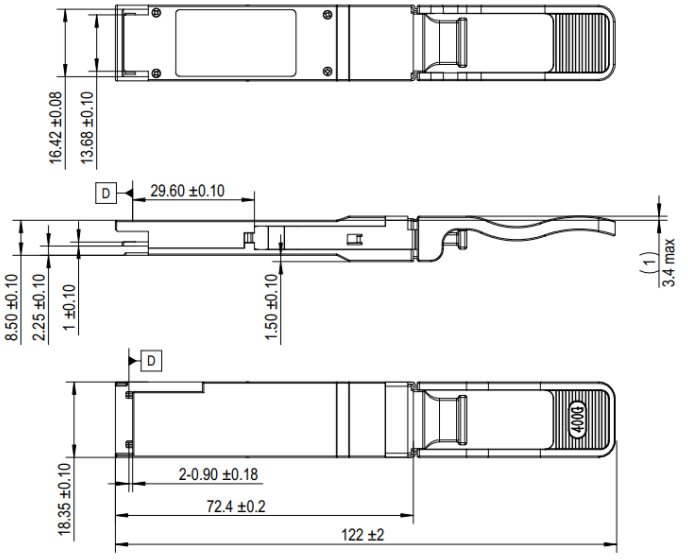


Figure 3. Optical lane assignments

13. Mechanical Specifications



Jnit : mm

Figure 4. Mechanical Dimensions

14. Ordering Information

Part Number	Description
WTF4XSR4CS1-XX	QSFP112 400G SR4 Optical Transceiver

XX: customized; 01 means Wiitek standard product